National Semiconductor

LP5952
350mA Dual Rail Linear Regulator

General Description

The LP5952 is a Dual Supply Rail Linear Regulator optimized for powering ultra-low voltage circuits from a single Li-Ion cell or 3 cell NiMH/NiCd batteries.

In the typical post regulation application V_{BATT} is directly connected to the battery (range 2.5V...5.5V) and V_{IN} is supplied by the output voltage of the DC-DC Converter (range 0.7V... 4.5V).

The device offers superior dropout and transient features combined with very low quiescent currents. In shutdown mode (Enable pin pulled low) the device turns off and reduces battery consumption to 0.1µA (typ.).

The LP5952 also features internal protection against over-temperature, over-current and under-voltage conditions.

Performance is specified for a -40°C to 125°C junction temperature range.

The device is available in a tiny 5-bump micro SMD and a 6-pin Chip On Lead LLP package, lead free.

The device is available in fixed output voltages in the range of 0.5V to 2.0V. For availability, please contact your local NSC sales office.

Features

- Excellent load transient response: ±15mV typical
- Excellent line transient response: ±1mV typical
- $0.7V \le V_{IN} \le 4.5V$
- $2.5V \le V_{BATT} \le 5.5V$
- $0.5V \le V_{OUT} \le 2.0V$
- For I_{LOAD} = 350mA: $V_{BATT} \ge V_{OUT(NOM)}$ + 1.5V or 2.5V whichever is higher
- For I_{LOAD} = 150mA: $V_{BATT} \ge V_{OUT(NOM)}$ + 1.3V or 2.5V whichever is higher
- 50µA typical quiescent current from V_{BATT}
- 10µA typical quiescent current from V_{IN}
- 0.1µA typical quiescent current in shutdown
- Guaranteed 350mA output current
- Noise voltage = 100µV_{RMS} typical
- Operates from a single Li-Ion cell or 3 cell NiMH/NiCd batteries
- Only one or two tiny surface-mount external components required depending on application
- Small, thin 5-bump micro SMD package and 6-pin Chip On Lead LLP package, lead free
- Thermal-overload and short-circuit protection
- -40°C to +125°C junction temperature range

Applications

- Mobile Phones
- Hand-Held Radios
- Personal Digital Assistants
- Palm-Top PCs
- Portable Instruments
- Battery Powered Devices

Typical Application Circuit

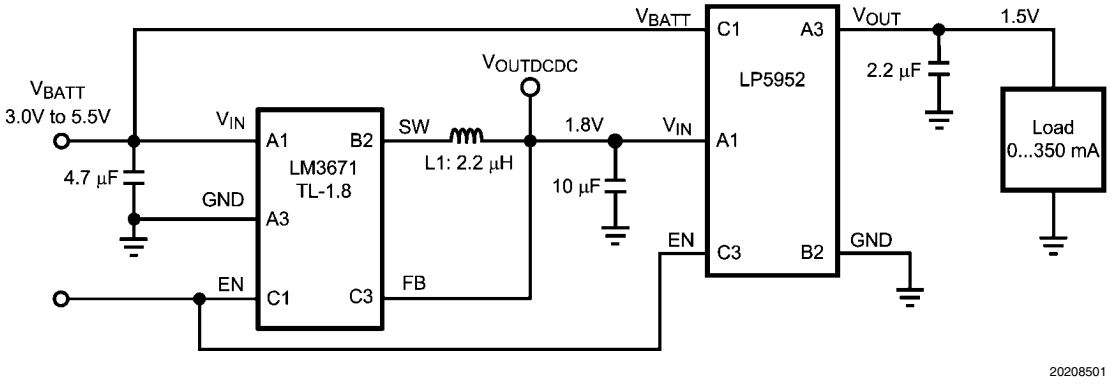
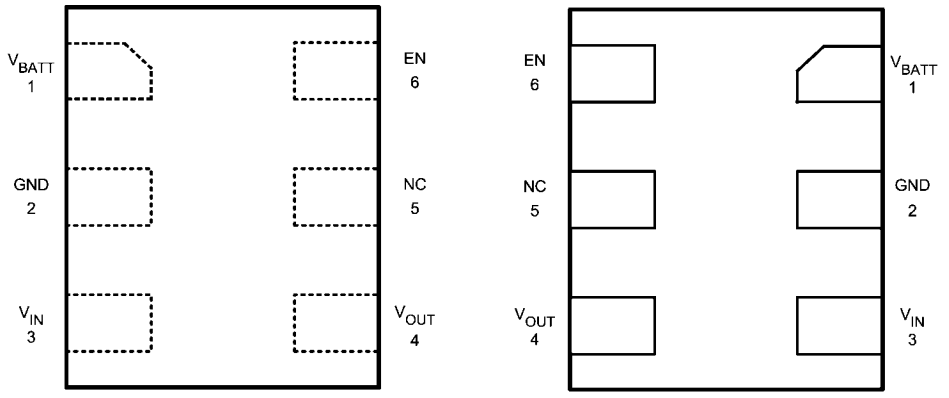


FIGURE 1. Typical Application Circuit with DC-DC Converter as Pre-Regulator for V_{IN}

LLP-6 Package



Connection Diagram 6-Pin Chip On Lead LLP package, 0.5mm pitch
See NS Package Number LCA06B

Note: The actual physical placement of the package marking will vary from part to part. The package marking "X" designates the date code. "T" is a NSC internal code for die traceability. Both will vary considerably. "U" identifies the device (part number, option, etc.).

Pin Descriptions

Pin Number Micro SMD	Pin Number LLP	Pin Name	Description
A1	3	V_{IN}	Power input voltage; input range: 0.7V to 4.5V, $V_{IN} \leq V_{BATT}$
A3	4	V_{OUT}	Regulated output voltage
B2	2	GND	Ground
C1	1	V_{BATT}	Bias input voltage; input range: 2.5V to 5.5V
C3	6	EN	Enable pin logic input: low = shutdown, high = active, normal operation. This pin should not be left floating. Tie to V_{BATT} if this function is not used.
	5	NC	Do not make connections to this pin

Order Information (5-bump micro SMD)

Output Voltage (V)	LP5952 Supplied as 250 Units, Tape and Reel, lead free	LP5952 Supplied as 3000 Units, Tape and Reel, lead free	Flow	Package Marking
0.7	LP5952TL-0.7	LP5952TLX-0.7	NOPB	4
1.0	LP5952TL-1.0	LP5952TLX-1.0	NOPB	L
1.2	LP5952TL-1.2	LP5952TLX-1.2	NOPB	7
1.3	LP5952TL-1.3	LP5952TLX-1.3	NOPB	U
1.4	LP5952TL-1.4	LP5952TLX-1.4	NOPB	A
1.5	LP5952TL-1.5	LP5952TLX-1.5	NOPB	T
1.6	LP5952TL-1.6	LP5952TLX-1.6	NOPB	B
1.8	LP5952TL-1.8	LP5952TLX-1.8	NOPB	8
2.0	LP5952TL-2.0	LP5952TLX-2.0	NOPB	5

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{IN}, V_{BATT} pins: Voltage to GND, $V_{IN} \leq V_{BATT}$:	-0.2V to 6.0V
V_{BATT} pin to V_{IN} pin:	0.2V
EN pin, Voltage to GND:	-0.2V to 6.0V
Continuous Power Dissipation (Note 3):	Internally Limited
Junction Temperature (T_{J-MAX}):	150°C
Storage Temperature Range:	-65°C to + 150°C
Package Peak Reflow Temperature (Pb-free, 10-20 sec.) (Note 4):	260°C
ESD Rating (Note 5):	
Human Body Model:	2.0kV
Machine Model:	200V

Operating Ratings

Input Voltage Range V_{IN}	0.7V to 4.5V
Input Voltage Range V_{BATT}	2.5V to 5.5V
V_{EN} Input Voltage	0 to V_{BATT}
Recommended Load Current	0mA to 350mA
Junction Temperature (T_J) Range	-40°C to + 125°C
Ambient Temperature (T_A) Range (Note 6)	-40°C to + 85°C

Thermal Properties

Junction-to-Ambient Thermal Resistance (θ_{JA})	
TLA05 package (Note 7)	95°C/W
LCA06B package (Note 7)	150°C/W

ESD Caution Notice

National Semiconductor recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper ESD handling techniques can result in damage.

Electrical Characteristics (Notes 2, 8, 11)

Typical values and limits appearing in standard typeface are for T_A = 25°C. Limits appearing in **boldface** type apply over the full operating temperature range: -40°C ≤ T_J ≤ +125°C. Unless otherwise noted, specifications apply to the typical application circuit with $V_{IN} = V_{OUT(NOM)} + 1.0V$, $V_{BATT} = V_{OUT(NOM)} + 1.5V$ or 2.5V, whichever is higher, I_{OUT} = 1mA, C_{VIN} = 1.0µF, C_{OUT} = 2.2µF, $V_{EN} = V_{BATT}$.

Symbol	Parameter	Condition	Typ	Limit		Units
				Min	Max	
$\Delta V_{OUT} / V_{OUT}$	Output Voltage Tolerance	$V_{IN} = V_{OUT(NOM)} + 0.3V$		-1.5 **-2.0**	1.5 **2.0**	% %
$\Delta V_{OUT} / \Delta V_{IN}$	Line Regulation Error	$V_{IN} = V_{OUT(NOM)} + 0.3V$ to 4.5V, V_{BATT} = 4.5V	0.3		**1.0**	mV/V
$\Delta V_{OUT} / \Delta V_{BATT}$		$V_{BATT} = V_{OUT(NOM)} + 1.5V$ (≥ 2.5V) to 5.5V	0.5		**2.2**	
$\Delta V_{OUT} / \Delta mA$	Load Regulation Error	I_{OUT} = 1mA to 350mA, micro SMD package	15		**30**	µV/mA
		I_{OUT} = 1mA to 350mA, LLP-6 package	43		**60**	µV/mA
I_{SC}	Output Current (short circuit)	V_{OUT} = 0V, $V_{EN} = V_{IN} = V_{BATT} = V_{OUT(NOM)} + 1.5V$	500	**350**		mA
V_{DO_VBATT} (Note 10)	Output Voltage Dropout V_{BATT} (Note 9)	I_{OUT} = 350mA, $V_{IN} = V_{OUT(NOM)} + 0.3V$, micro SMD package	1.07		**1.5**	V
		I_{OUT} = 350mA, $V_{IN} = V_{OUT(NOM)} + 0.3V$, LLP-6 package	1.08		**1.5**	V
		I_{OUT} = 150mA, $V_{IN} = V_{OUT(NOM)} + 0.3V$, micro SMD package	0.96		**1.3**	V
		I_{OUT} = 150mA, $V_{IN} = V_{OUT(NOM)} + 0.3V$, LLP-6 package	0.97		**1.3**	V
V_{DO_VIN}	Output Voltage Dropout V_{IN}	I_{OUT} = 350mA, $V_{BATT} = V_{OUT(NOM)} + 1.5V$ or 2.5V, micro SMD package	88		**200**	mV
		I_{OUT} = 350mA, $V_{BATT} = V_{OUT(NOM)} + 1.5V$ or 2.5V, LLP-6 package	128		**250**	mV
E_N	Output Noise	10Hz to 100kHz	100			μV_{RMS}

Symbol	Parameter	Condition	Typ	Limit		Units
				Min	Max	
PSRR	Power Supply Rejection Ratio	Sine modulated V_{BATT}				
		f = 10Hz	70			dB
		f = 100Hz	65			dB
		f = 1kHz	45			dB
		Sine modulated V_{IN}				
		f = 10Hz	80			dB
		f = 100Hz	90			dB
		f = 1kHz	95			dB
		f = 10kHz	85			dB
		f = 100kHz	64			dB

Quiescent Currents

Symbol	Parameter	Condition	Typ	Limit		Units
				Min	Max	
I_{Q_VBATT}	Current into V_{BATT}	I_{LOAD} = 0...350mA	50		**100**	µA
I_{Q_VIN}	Current into V_{IN}	I_{LOAD} = 0	11		**28**	µA

Shutdown Currents

Symbol	Parameter	Condition	Typ	Limit		Units
				Min	Max	
I_{Q_VBATT}	Current into V_{BATT}	V_{EN} = 0V	0.1		**1**	µA
I_{Q_VIN}	Current into V_{IN}	V_{EN} = 0V	0.1		**1**	µA

Enable Control Characteristics

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
I_{EN}	Maximum Input Current at V_{EN} Input		0.01		**1**	µA
V_{IL}	Low Input Threshold (shutdown)				**0.4**	V
V_{IH}	High Input Threshold (enable)			**1.0**		V

Thermal Protection

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
T_{SHDN}	Thermal-Shutdown Temperature		165			°C
ΔT_{SHDN}	Thermal-Shutdown Hysteresis		20			°C

Transient Characteristics

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
ΔV_{OUT}	Dynamic Line Transient Response V_{IN}	$V_{IN} = V_{OUT(NOM)} + 0.3V$ to $V_{OUT(NOM)} + 0.9V$; tr, tf = 10µs	±1			mV
ΔV_{OUT}	Dynamic Line Transient Response V_{BATT}	$V_{BATT} = V_{OUT(NOM)} + 1.5V$ to $V_{OUT(NOM)} + 2.1V$; tr, tf = 10µs	±15			mV
ΔV_{OUT}	Dynamic Load Transient Response	Pulsed load 0 ...300mA, di/dt = 300mA/1µs micro SMD package	±15			mV
		Pulsed load 0 ...300mA, di/dt = 300mA/1µs LLP-6 package	-35/+15			mV
$T_{STARTUP}$	Startup Time	EN to 0.95 * V_{OUT}	70		**150**	µs

Input and Output Capacitors, Recommended Specification

Symbol	Parameter	Conditions	Nom	Limit		Units
				Min	Max	
C_{OUT}	Output Capacitance	Capacitance (Note 12)	2.2	1.5	10	µF
		ESR		3	300	mΩ
C_{VIN}	Input Capacitance at V_{IN}	Capacitance (Note 12), not needed in typ post regulation application, see *Figure 1*	1	0.47		µF
		ESR		3	300	mΩ

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: All voltages are with respect to the potential at the GND pin.

Note 3: Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 165°C (typ.) and disengages at T_J = 145°C (typ.).

Note 4: For detailed soldering specifications and information, please refer to National Semiconductor Application Note 1112: Micro SMD Wafer Level Chip Scale Package (AN-1112) and Application Note 1187: Leadless Leadframe Package (LLP) (AN-1187).

Note 5: The Human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin. (MIL-STD-883 3015.7)

Note 6: In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (\theta_{JA} \times P_{D-MAX})$.

Note 7: Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special attention must be paid to thermal dissipation issues in board design.

Note 8: Min and Max limits are guaranteed by design, test, or statistical analysis. Typical (Typ) numbers are not guaranteed, but do represent the most likely norm. Unless otherwise specified, conditions for Typ specifications are: $V_{IN} = V_{OUT(NOM)} + 1.0V$, $V_{BATT} = V_{OUT(NOM)} + 1.5V$ or 2.5V, whichever is higher, T_A = 25° C.

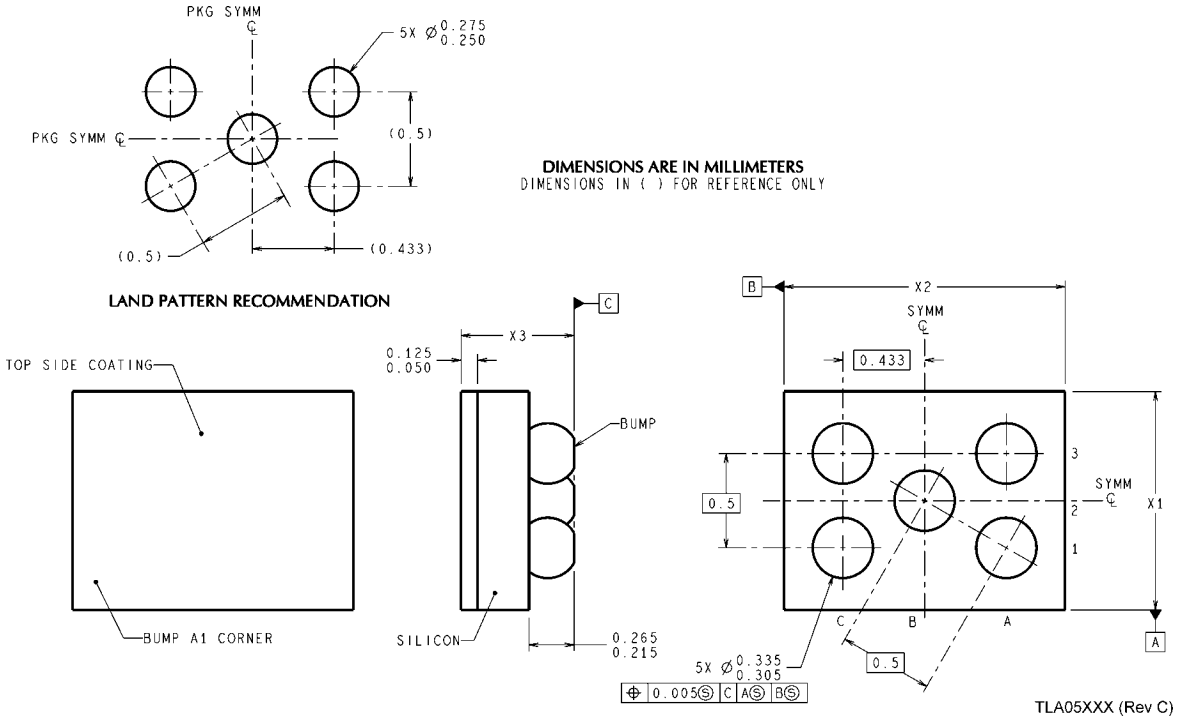
Note 9: Dropout voltage is defined as the input to output voltage differential at which the output voltage falls to 100mV below the nominal output voltage.

Note 10: This specification does not apply if the battery voltage V_{BATT} needs to be decreased below the minimum operating limit of 2.5V during this test.

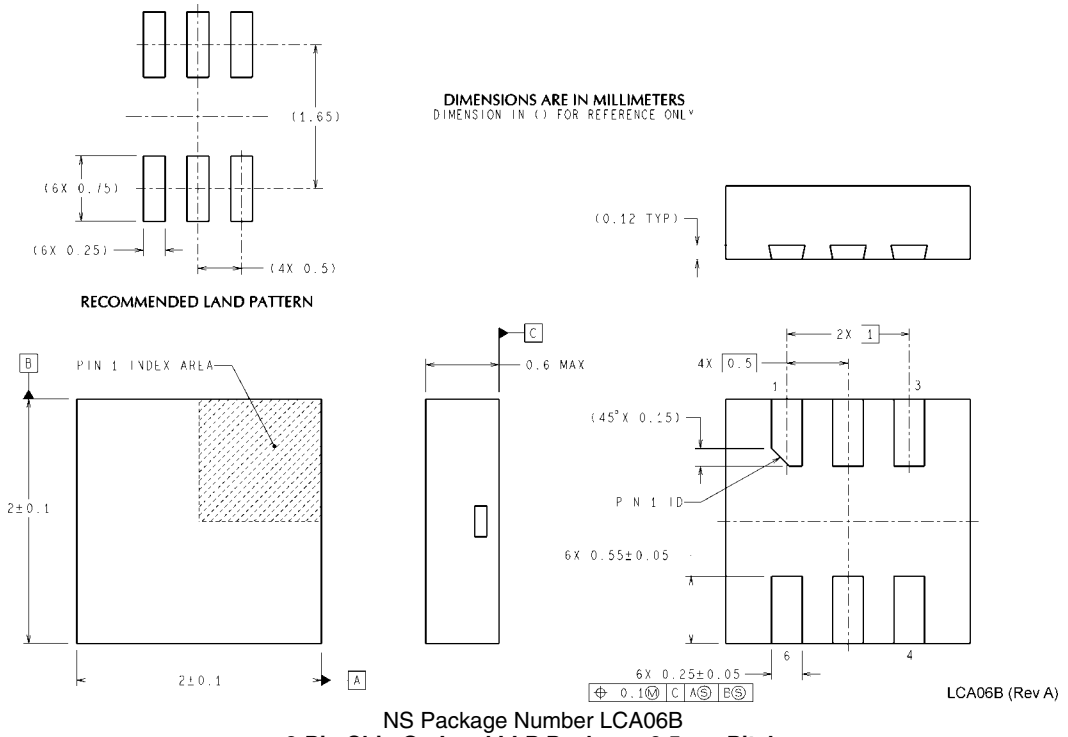
Note 11: $V_{OUT(NOM)}$ is the stated output voltage option

Note 12: The capacitor tolerance should be 30% or better over temperature. The full operating conditions for the application should be considered when selecting a suitable capacitor to ensure that the minimum value of capacitance is always met. Recommended capacitor type is X7R. However, dependent on application, X5R, Y5V, and Z5U can also be used. The shown minimum limit represents real minimum capacitance, including all tolerances and must be maintained over temperature and dc bias voltage (See capacitor section in Applications Hints)

Physical Dimensions inches (millimeters) unless otherwise noted



NS Package Number TLA05Z1A
X1 = 955 µm ±30µm
X2 = 1335µm ±30µm
X3 = 600µm ±75µm
5-Bump Thin Micro SMD Package, Large Bump



NS Package Number LCA06B
6-Pin Chip On Lead LLP Package, 0.5mm Pitch

For most accurate revision please refer to www.national.com/packaging/parts/